REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to military drawing format. Changed OE to $\overline{OE}$ in figures 1, 2, and 3. Correction in vendor similar part number. Editorial changes throughout.	88 MAY 25	D. R. Cool

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	A	A																		
SHEET	15	16																		

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
ASHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
Charles Reusing

APPROVED BY
D. R. Cool

DRAWING APPROVAL DATE
10 OCTOBER 1985

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, BIPOLAR, PROGRAMMABLE, LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**14933**	**85065**

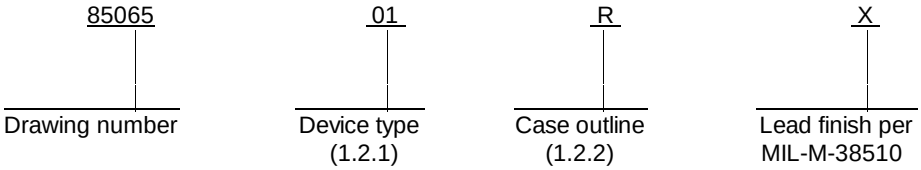
SHEET 1 OF 16

*** US GOVERNMENT PRINTING OFFICE: 1987--748-129/60912**
5962-E852

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	PAL16L8A-4	16-input 8-output AND-OR invert gate array
02	PAL16R8A-4	16-input 8-output registered AND-OR gate array
03	PAL16R6A-4	16-input 6-output registered AND-OR gate array
04	PAL16R4A-4	16-input 4-output registered AND-OR gate array

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range -0.5 V dc to +12.0 V dc
Input voltage range -1.5 V dc to +5.5 V dc
Storage temperature range - - - - - - - - - - - - - - - - - -65°C to +150°C
Lead temperature (soldering, 10 seconds) - - - - - - +260°C
Thermal resistance, junction-to-case (O_{JC}): 1/
Cases R, S, and 2 - See MIL-M-38510, appendix C
Output voltage applied -1.5 V dc to +12 V dc
Output sink current- 100 mA
Maximum power dissipation (P_D) 2/
Device types 01, 02, 03, and 04 - - - - - - - - - - - - 300 mW
Maximum junction temperature (T_J)- - - - - - - - - - - +175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - 4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}) - - - - - - - - 2.0 V dc
Maximum low level input voltage (V_{IL}) - - - - - - - - - 0.8 V dc
Case operating temperature range (T_C) - - - - - - - - -55°C to +125°C

1/ Heat sinking is recommended to reduce the junction temperature.
2/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, or C (see 4.3.1c), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of gates programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Unprogrammed logic diagram. The unprogrammed logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

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3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.5.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.5.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing shall be satisfied by the manufacturer prior to delivery.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS}=0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A sub-groups	Device type	Limits		Unit
					Min	Max	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_I = -18 mA	1, 2, 3	All		-1.5	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V, $V_{IL} \le$ 0.8 V $V_{IH} \ge$ 2 V, I_{OH} = -1 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, $V_{IL} \le$ 0.8 V $V_{IH} \ge$ 2 V, I_{OL} = 4 mA	1, 2, 3	All		0.5	V
High level input voltage	V_{IH}	V_{CC} = 5.5 V 1/	1, 2, 3	All	2		V
Low level input voltage	V_{IL}	V_{CC} = 5.5 V 1/	1, 2, 3	All		0.8	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_I = 2.4 V 2/	1, 2, 3	All		25	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_I = 0.4 V 2/	1, 2, 3	All		-0.25	mA
Output short circuit current	I_{OS}	V_{CC} = 5 V, V_O = O V 3/	1, 2, 3	All	-30	-130	mA
Input current	I_I	V_{CC} = 5.5 V, V_I = 5.5 V	1, 2, 3	All		1.0	mA
Off state output current	I_{OZL}	V_{CC} = 5.5 V, $V_{IL} \le$ 0.8 V $V_{IH} \ge$ 2.4 V, V_O = 0.4 V 2/	1, 2, 3	All		-100	µA
Off state output current	I_{OZH}	V_{CC} = 5.5 V, $V_{IL} \le$ 0.8 V $V_{IH} \ge$ 2.4 V, V_O = 2.4 V 2/	1, 2, 3	All		100	µA
Supply current	I_{CC}	V_{CC} = 5.5 V	1, 2, 3	All		50	mA
Propagation delay data input to output	t_{PHL}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_1 = 800Ω, R_2 = 1.56 kΩ	9,10,11	01, 03, 04		75	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS}=0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A sub-groups	Device type	Limits Min	Limits Max	Unit
Propagation delay data input to output	t_{PLH}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_1 = 800Ω, R_2 = 1.56kΩ	9,10,11	01, 03, 04		75	ns
Propagation delay output high impedance to output high	t_{PZH1}		9,10,11	01, 03, 04		65	ns
Propagation delay output high impedance to output low	t_{PZL1}		9,10,11	01, 03, 04		65	ns
Propagation delay output high to output high impedance	t_{PHZ1}		9,10,11	01, 03, 04		65	ns
Propagation delay output low to output high impedance	t_{PLZ1}		9,10,11	01, 03, 04		65	ns
Propagation delay high impedance to output high (pin 11 to output enable) 4/	t_{PZH2}		9,10,11	02, 03, 04		40	ns
Propagation delay high impedance to output low (pin 11 to output enable) 4/	t_{PZL2}		9,10,11	02, 03, 04		40	ns
Propagation delay output high to high impedance (pin 11 to output disable) 4/	t_{PHZ2}		9,10,11	02, 03, 04		40	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS}=0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Group A sub-groups	Device type	Limits Min	Limits Max	Unit
Propagation delay output low to high impedance (pin 11 to output disable) 4/	t_{PLZ2}	V_{CC} = 5.0 V, C_L = 50 pF ±10% R_1 = 800Ω, R_2 = 1.56 kΩ	9,10,11	02, 03, 04		40	ns
Clock pulse width 4/ 5/	$t_{p(CL)}$		9,10,11	02, 03, 04	40		ns
Setup time 4/ 5/	t_{SU}		9,10,11	02, 03, 04	90		ns
Hold time 5/	t_H		9,10,11	All	0		ns
Maximum clock 4/ 5/	f_{MAX}		9,10,11	02, 03, 04	8		MHz

1/ These are absolute voltages with respect to the ground pin on the device and are subject to change depending on test hardware.

2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZX}.

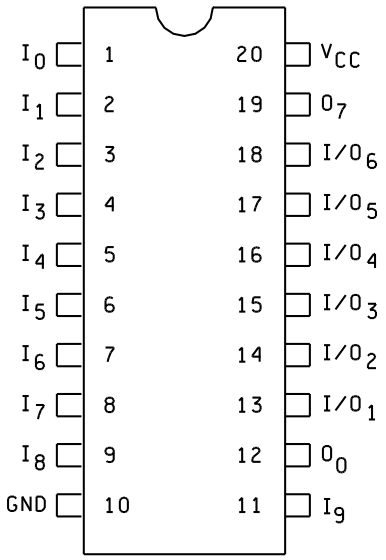
3/ Only one output shorted at a time.

4/ Test applies only to register outputs.

5/ Tested only initially and after any design changes.

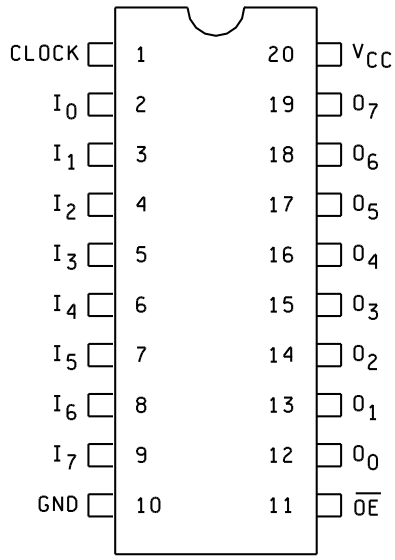
DEVICE TYPE 01

CASE R AND S



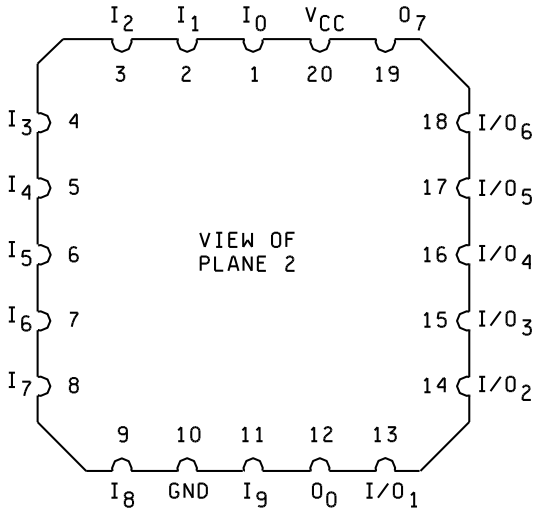
DEVICE TYPE 02

CASE R AND S



DEVICE TYPE 01

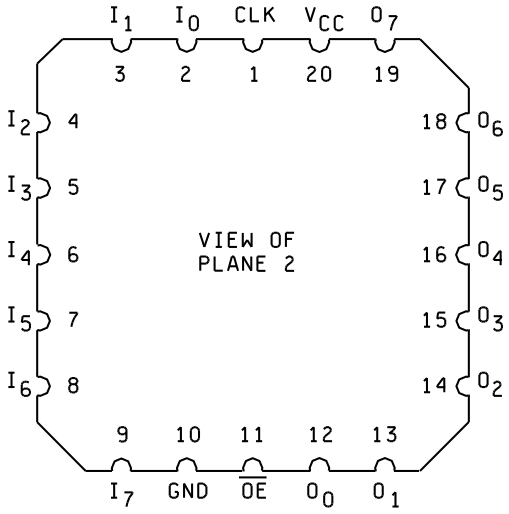
CASE 2



OPTION A WITH ACTIVE TERMINALS
ON PLAN 1.

DEVICE TYPE 02

CASE 2



OPTION A WITH ACTIVE TERMINALS
ON PLAN 1.

FIGURE 1. Terminal connections.

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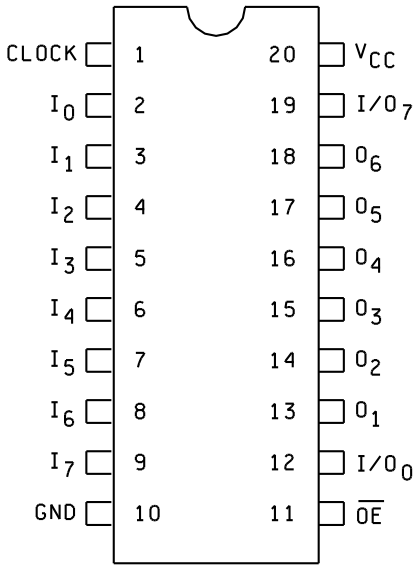
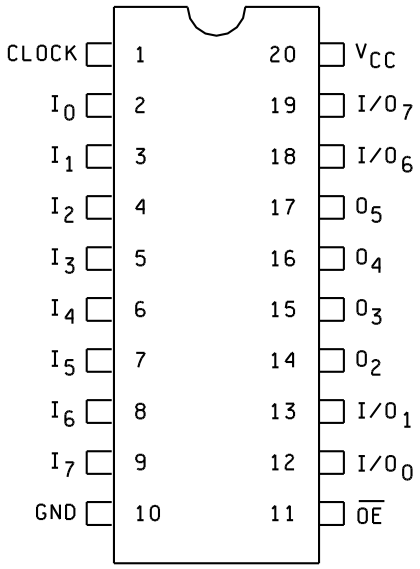
DEVICE TYPE 03

CASE R AND S



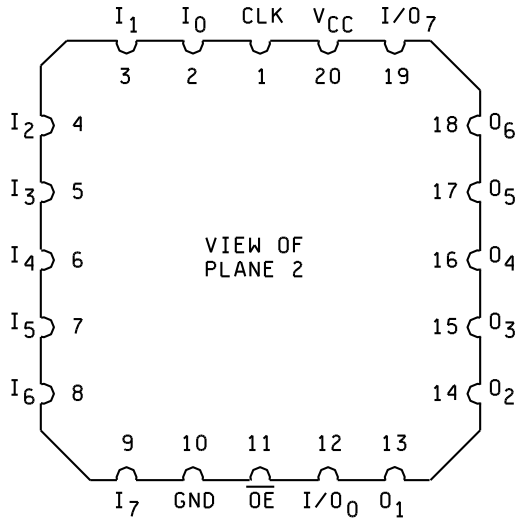
DEVICE TYPE 04

CASE R AND S



DEVICE TYPE 03

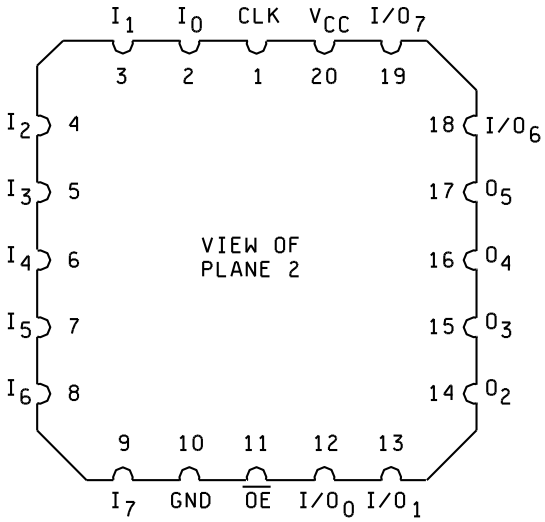
CASE 2



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

DEVICE TYPE 04

CASE 2



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

FIGURE 1. Terminal connections - Continued.

Truth table																				
Address												Output level								
CK	$\overline{OE}$	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	Device
		X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	01
CK	L			X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	02
CK	L			X	X	X	X	X	X	X	X	Z	H	H	H	H	H	H	Z	03
CK	L			X	X	X	X	X	X	X	X	Z	Z	H	H	H	H	Z	Z	04

NOTES:
1. Z = Three-state.
2. Clock (pin 1) - low to high transition required to obtain valid data after last address transition.
3. Enable (pin 11) - must be low to enable output.

FIGURE 2. Truth table (unprogrammed).

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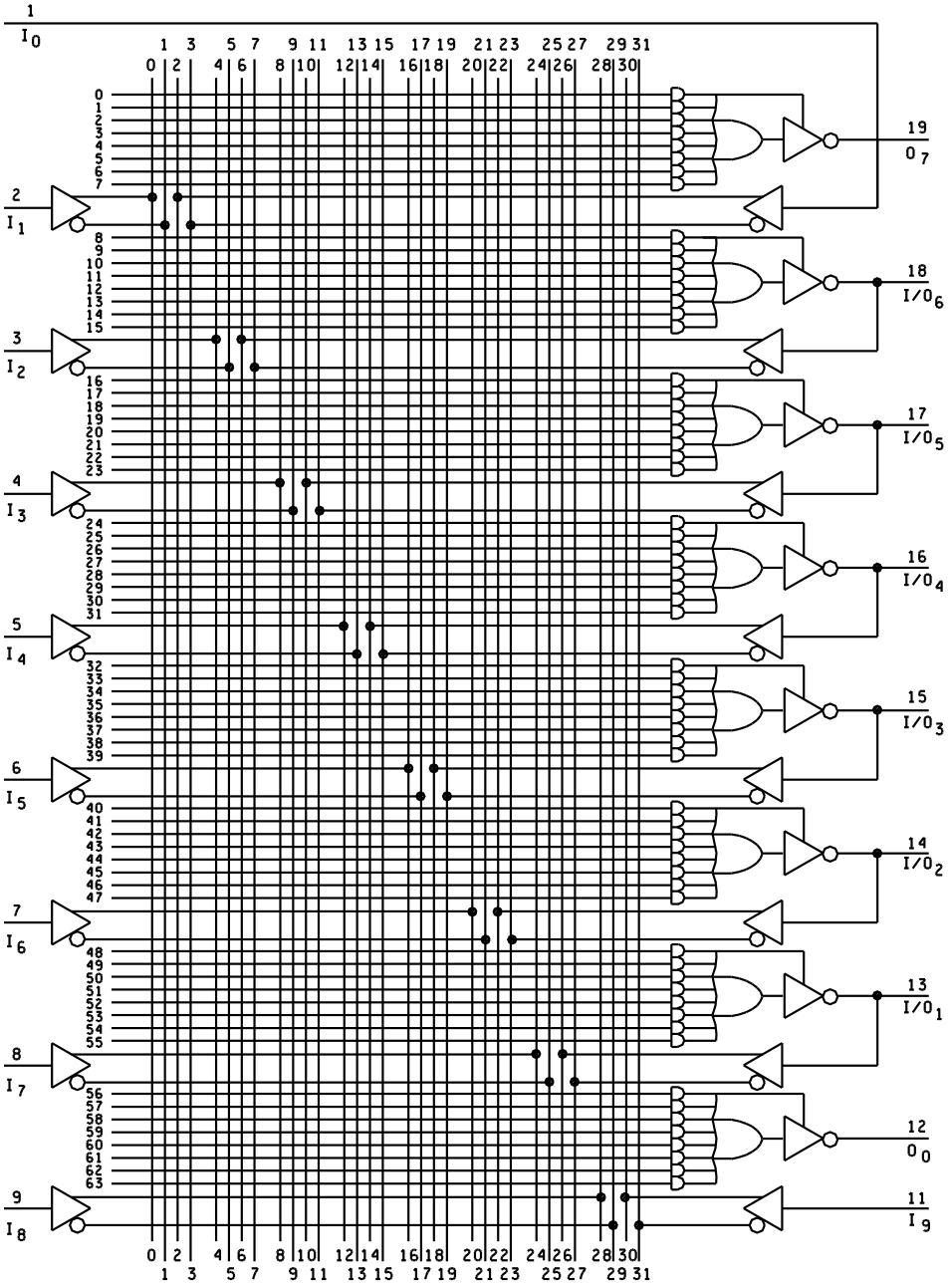
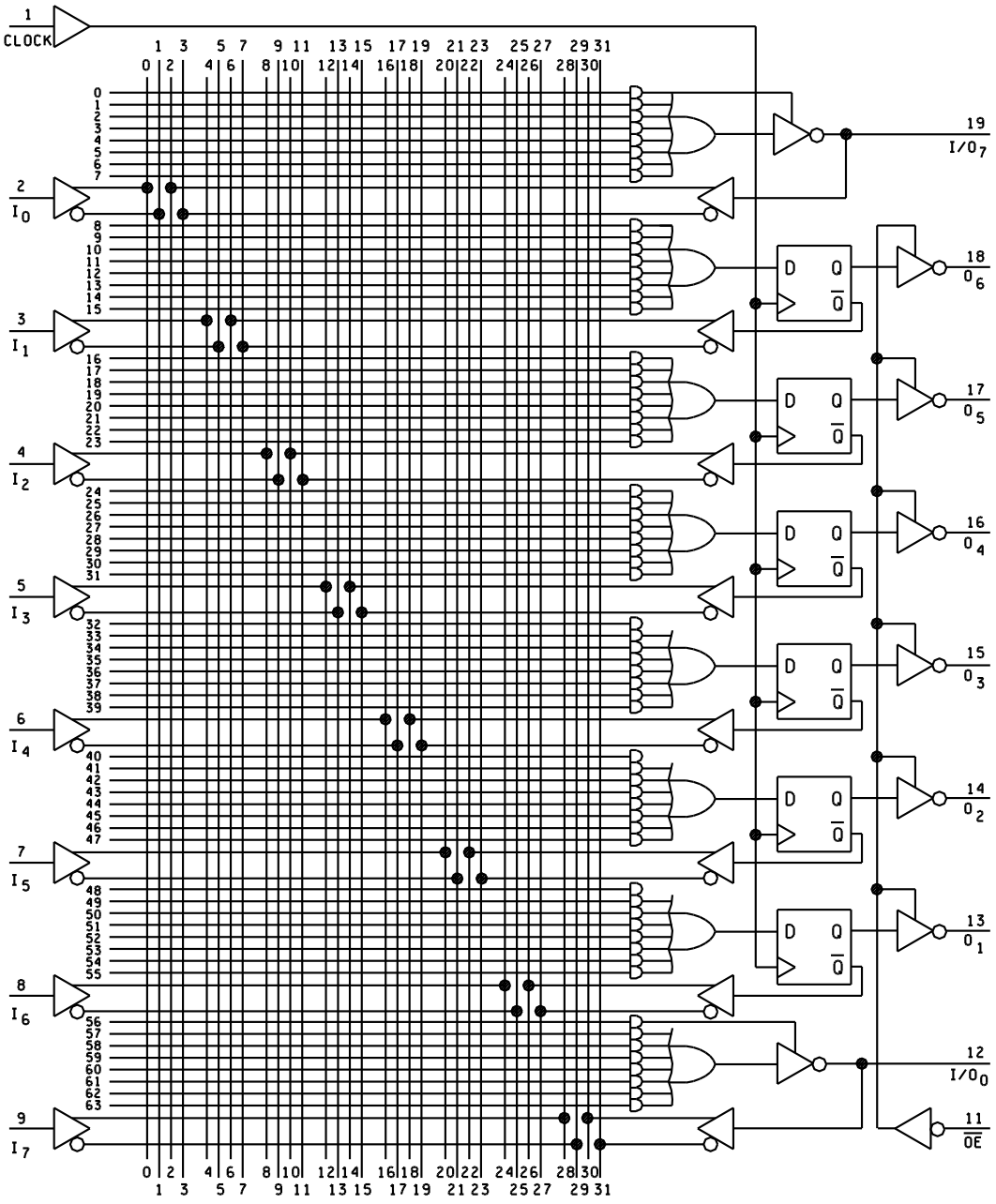
DEVICE TYPE 01



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram.

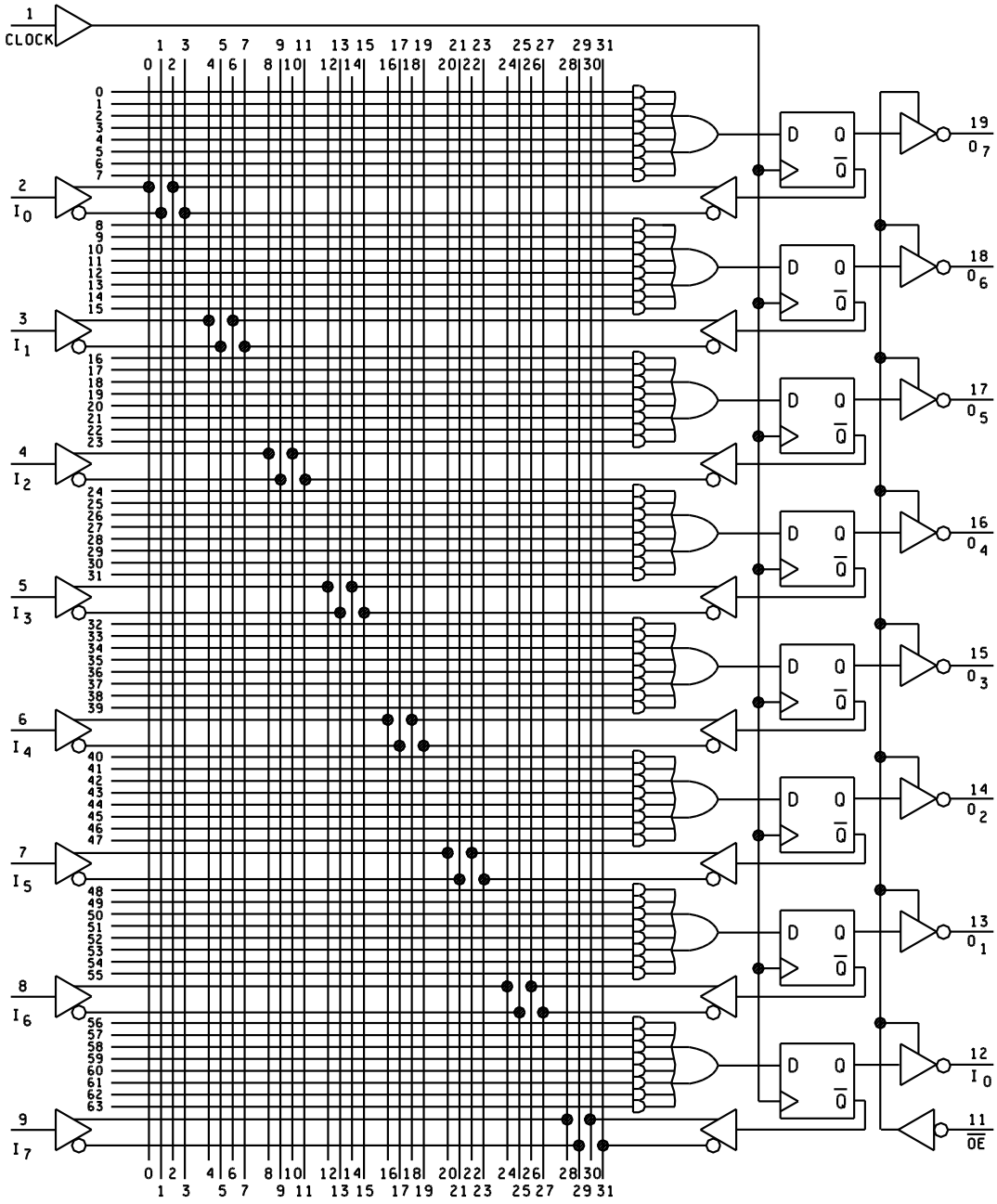
DEVICE TYPE 02



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

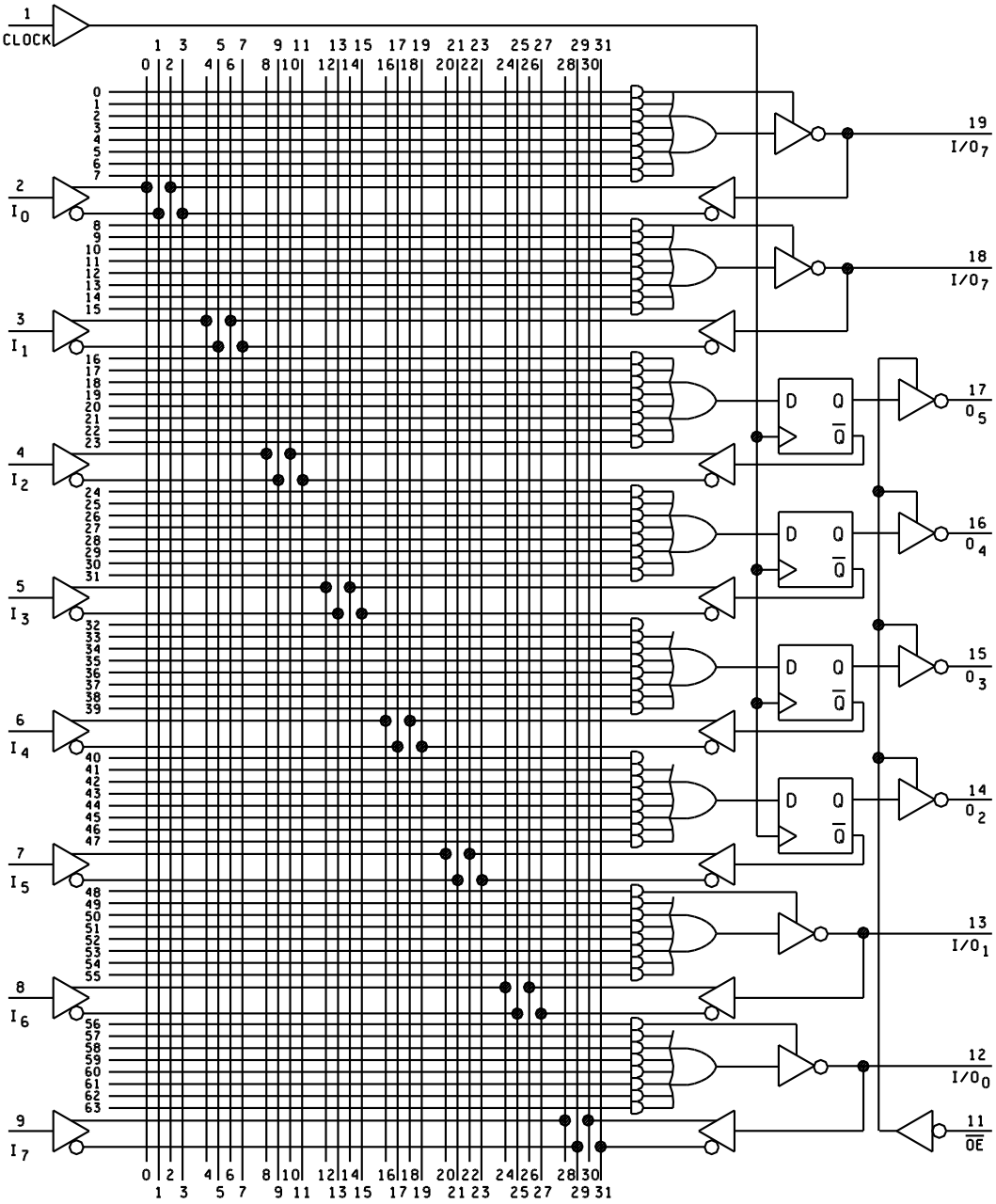
DEVICE TYPE 03



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

DEVICE TYPE 04



NOTE: EACH INTERSECTION OF NUMBERED LINES INDICATES A FUSIBLE LINK.

FIGURE 3. Unprogrammed logic diagram - Continued.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*, 2, 3, 7*, 8
Final electrical test parameters (method 5004) for programmed devices	1*, 2, 3, 7*, 8, 9
Group A test requirements (method 5005)	4/ 1, 2, 3, 7, 8, 9 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8

1/ (*) indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high speed testers.
3/ Subgroups 7 and 8 functional tests shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For unprogrammed devices, a sample shall be selected to satisfy programmability requirements prior to performing subgroup 9. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

d. For unprogrammed devices, ten devices from the programmability sample shall be submitted to the requirements of group A, subgroup 9. If more than two total devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
8506501RX	50364	PAL16L8A-4MJ/883B
8506501SX	50364	PAL16L8A-4MW/883B
85065012X	50364	PAL16L8A-4ML/883B
8506502RX	50364	PAL16R8A-4MJ/883B
8506502SX	50364	PAL16R8A-4MW/883B
85065022X	50364	PAL16R8A-4ML/883B
8506503RX	50364	PAL16R6A-4MJ/883B
8506503SX	50364	PAL16R6A-4MW/883B
85065032X	50364	PAL16R6A-4ML/883B
8506504RX	50364	PAL16R4A-4MJ/883B
8506504SX	50364	PAL16R4A-4MW/883B
85065042X	50364	PAL16R4A-4ML/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Fusible link
50364	Monolithic Memories, Inc. 2175 Mission College Blvd. Santa Clara, CA 95051	Titanium-Tungsten